

#17 / Response
(PE)

1/15/03

Shan H

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

HENRY CHUNG

Docket: 30-4718 (4780)

Serial Number: 09/328,645

Group Art Unit: 2811

Filed: June 9, 1999

Examiner: H. Vu

For: A FABRICATION METHOD OF INTEGRATED CIRCUITS WITH
BORDERLESS VIAS AND LOW DIELECTRIC-CONSTANT INTER-METAL
DIELECTRICS

NOTICE: THIS APPLICATION IS UNDER FINAL REJECTIONRESPONSE TO OFFICE ACTION

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Commissioner for Patents
Washington, D.C. 20231

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Sir:

In response to the Office Action mailed December 4, 2002, please consider the following
remarks:

REMARKS

The examiner has rejected claims 5-7 under 35 U.S.C. 102 over Lu et al. Applicants
respectfully assert that this ground of rejection is improper.

The present invention relates to the formation of borderless vias in intermetal dielectrics.

The invention claims an integrated circuit structure which comprises:

- (a) a substrate;
- (b) a layer of a first polymeric dielectric material on the substrate;
- (c) a plurality of spaced apart metal contacts on the layer of the first polymeric
dielectric material;
- (d) a space between adjacent metal contacts, each space being filled with a second
polymeric dielectric material;

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DATE: January 6, 2003

KINDLY DIRECT THIS COMMUNICATION TO:

EXAMINER : H. Vu
GROUP : 2811

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